UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/722,652 | 11/26/2003 | Kerry Leeds Davison | 4-7-23 | 7648 |

7590 03/13/2006

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

| EXAMINER | |
|---|---|
| NGO, HUNG V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2831 | |

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**



Application Number: 10/722,652
Filing Date: November 26, 2003
Appellant(s): DAVISON ET AL.

Robert W. Griffith
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 10-17-05 appealing from the Office action mailed 01-26-05.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of claims**

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-8, 14, 15, 17-20.

Claims 1-8, 14, 15, 17-20 are rejected under 35 USC 102(e)

Claims 9-13, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

Claims 1-8, 14, 15, 17-20 are rejected under 35 USC 102(e) as being anticipated by US Pat. No 6,727,597 to Taylor et al.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 6,727,597 | Taylor et al | 04-2004 |
| Exhibit A | Fig 3B of Taylor et al | |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 14, 15, 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor et al (US 6,727,597).

Re claim 1,Taylor et al disclose an integrated circuit device comprising:

a die (300) having a top surface with a peripheral region and an interior region surrounded by the peripheral region:

a plurality of bond pads (304, 350 and other adjacent pads in Fig 3b) disposed in the peripheral region of the die;

at least one internal bus (positive power bus 360, negative/ground bus 362), disposed in the interior region of the die, for distributing power to a plurality of internal node points of the die (Fig 3b); and

at least one bond wire connecting at least one of the plurality of bond pads with the at least one internal bus (Fig 3b).

Re claim 2. The integrated circuit device of claim 1, wherein the at least one internal bus comprises a metal power grid (360)(col. 3, line 18).

Re claim 3, wherein the at least one internal bus comprises at least one internal positive voltage supply bus (360)(col. 3, line 18).

Re claim 4, wherein the at least one internal bus comprises at least one internal negative voltage supply bus (negative/ground bus 362) (col. 3, line 22).

Re claim 5, wherein the at least one internal bus comprises at least one pair of buses comprising an internal positive voltage (360) supply bus and internal negative voltage supply bus (negative/ground bus 362) (col. 3, line 22).

Re claim 6, wherein at least one of the voltage supply buses comprises a ground bus (negative/ground bus 362) (col. 3, line 22).

Re claim 7, wherein the at least one internal bus (360, 362) comprises bond pads (Fig 3b) having active circuitry disposed thereunder (Fig 3c).

Re claim 8, wherein at least one of the plurality of bond pads is wire bonded to an integrated circuit package (360)(Fig 3c)(col. 2, line 51).

Re claim 14, further comprising local power interconnects (340) that distribute power from the at least one internal bus to the plurality of internal node points (Fig 3b).

Re claim 15, wherein the plurality of internal node points comprise circuit elements (Fig 3b).

Re claim 17, wherein the at least one of the plurality of bond pads comprises at least one pair of bond pads comprising a positive voltage supply bond pad (340) and a negative voltage supply bond pad (342).

Re claim 18, wherein the at least one pair of bond pads comprises at least about twelve pairs of bond pads substantially evenly spaced apart in the peripheral region of the die (Fig 3b).

Re claim 19, Taylor et al disclose die (300) configurable for use in an integrated circuit device, the die having a top surface with a peripheral region and an interior region surrounded by the peripheral region, the die comprising:

a plurality of bond pads (304, 350 and other adjacent pads in Fig 3b) disposed in the peripheral region of the die; and

at least one internal bus (positive power bus 360, negative/ground bus 362), disposed in the interior region of the die, that distributes power to a plurality of internal node points of the die (Fig 3b);

wherein, the plurality of bond pads and the at least one internal bus are connectable by at least one bond wire (Fig 3b).

Re claim 20, a method of constructing an integrated circuit device comprising the following steps:

forming an integrated circuit die (300) having at least one peripheral bond pad (304, 350 and other adjacent pads in Fig 3b) and at least one internal bus (positive power bus 360, negative/ground bus 362), the internal bus being configured for distributing power to a plurality of internal node points of the integrated circuit device (Fig 3b); and

wire bonding the at least one peripheral bond pad to the at least one internal bus (Fig 3b).

**(10) Response to Argument**

Appellant argues (1) that Taylor fails to disclose at least one bond wire connecting at least one of a plurality of bond pads, (2) that Taylor fails to disclose the step of wire bonding a peripheral bond pad to an internal bus, (3) that Taylor does not disclose a method of constructing an integrated circuit device.

With respect to (1) Taylor et al disclose at least one bond wire connecting at least one of a plurality of bond pads (304, 350 Fig 3b) (see Exhibit A), and Taylor et al recite "each c4 power bus 360 is electronically coupled to one or more wire bond pad power connections 350" (col. 3, lines 18-20).

With respect to (2) Taylor et al disclose the step of wire bonding a peripheral bond pad (304, 350) to an internal bus (positive power bus 360, negative/ground bus 362), see Exhibit A.

With respect to (3) Taylor et al disclose a method of constructing an integrated circuit device (abstract) comprising:

forming an integrated circuit die (300) having at least one peripheral bond pad (304, 350 and other adjacent pads in Fig 3b) and at least one internal bus (positive power bus 360, negative/ground bus 362), the internal bus being configured for distributing power to a plurality of internal node points of the integrated circuit device (Fig 3b); and

wire bonding the at least one peripheral bond pad to the at least one internal bus (Fig 3b) (col. 2, line 53 to col. 3, line 50).

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hung V Ngo

HUNG V. NGO
PRIMARY EXAMINER

Hung V Ngo

Conferees:

Dean Reichard DR

Darren Schuberg DS

Exhibit A

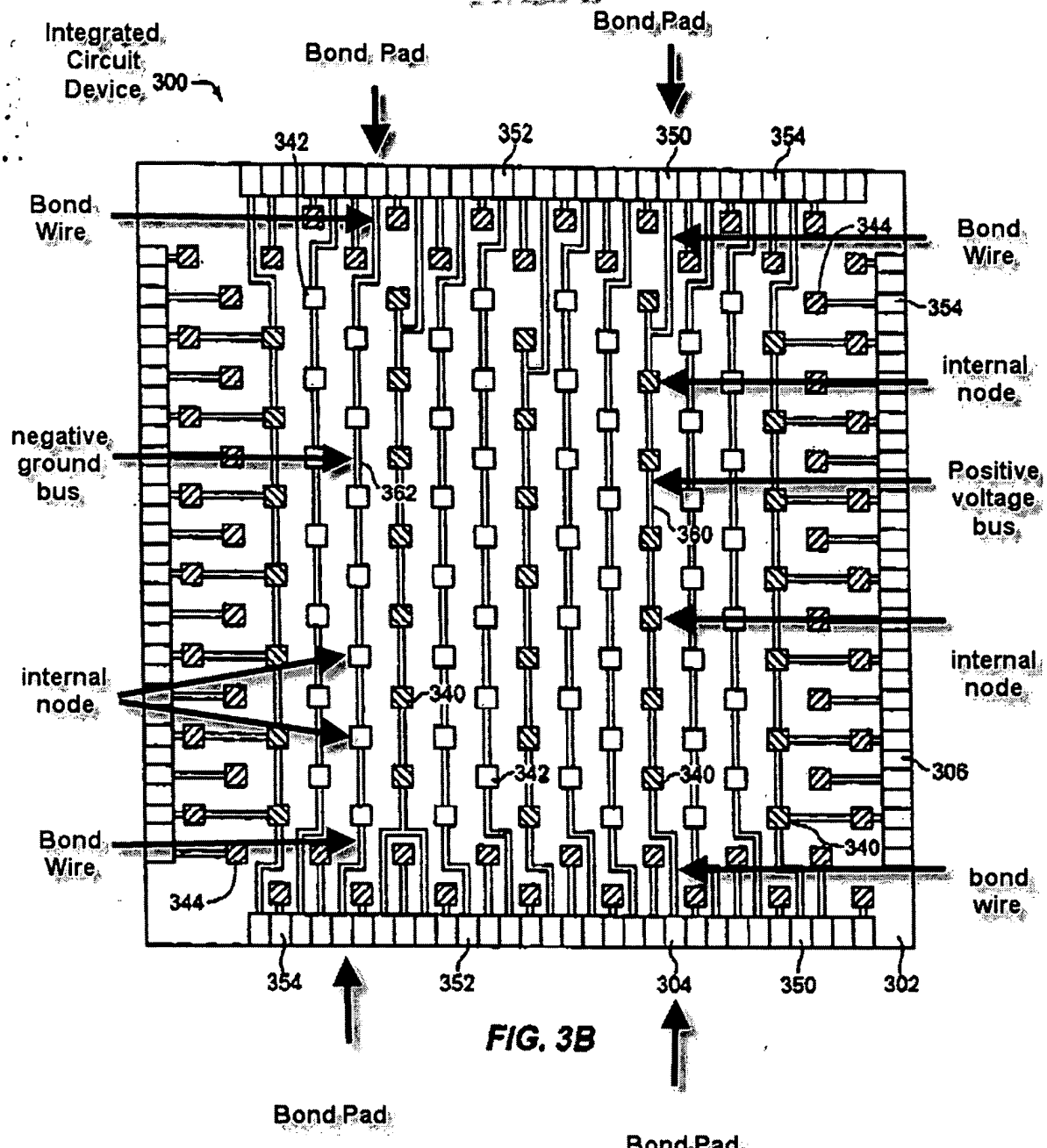


FIG. 3B